IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	T. Haze	Attorney Docket No.:	LEPA122745
Application No.:	10/823,297	Art Unit: 2822 / Confirmation No:	4560
Filed:	April 13, 2004	Examiner:	P.E. Perkins
Title:	METHOD OF FORMING BUMP PAD OF FLIP CHIP AND STRUCTURE THEREOF		

RESPONSE AFTER NON-FINAL REJECTION

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TO THE COMMISSIONER FOR PATENTS:

This paper is filed in response to the Office Action mailed on September 6, 2007. Presently, Claims 1-9 are pending in the application. Of these, Claims 7-9 are withdrawn from consideration. Claims 1-6 have been examined and stand rejected. Reconsideration of Claims 1-6 is respectfully requested.

The Rejection of Claims 1-6 Under 35 U.S.C. § 103(a)

Claims 1-6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Korean Patent Application No. 1020030072855 (Lee) in view of U.S. Patent No. 7,008,867 (Lei) and U.S. Patent Application Publication No. US 2004/0253804 (Beica et al.).

Claim 1 is directed to a method of forming a *bump pad*. A bump pad is the structure that resides on and is next to the substrate and below a bump. The method for forming the bump pad includes three layer–forming steps: (1) electroless copper plating to prepare an electroless copper plating layer on the substrate, (2) pulse plating on the electroless copper plating layer to prepare a pulse plating layer, and (3) electrolytic copper plating using a direct current on the pulse plating layer to prepare a direct current plating layer.

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As recited in Claim 1, the bump pad that is formed results in a bump pad having an electroless copper plated layer juxtaposed on an insulating layer, a pulse plated layer juxtaposed on the electroless copper plated layer, and a direct current copper plated layer juxtaposed on the pulse plated layer. That is, the method of Claim 1 results in a bump pad having three layers: 1) an electroless copper plated layer, 2) a pulse plated layer, and 3) a direct current copper plated layer. Because the bump pads that are described in Lei, Lee, and Beica do not resemble the bump pad that is formed by the method of Claim 1, the combination of references cannot teach nor suggest all the claimed steps of the method of Claim 1.

For example, from the figures in the Korean patent of Lee (copy enclosed), it appears that the bump pads 12 and 13 are made from a single layer. Furthermore, the English abstract clearly supports the proposition that Lee only has one layer in the bump pad. Lee discloses "a first copper plating step of electroless copper plating the solder ball land of a substrate having a via hole." Lee discloses that the second copper plating step is for *forming a lead wire* for interconnecting the circuit and the solder ball land. Therefore, this second step is not for forming part of the bump pad. Accordingly, Lei does not disclose a method for (1) pulse plating over the electroless copper layer nor (2) subjecting the pulse plating layer to electrolytic copper plating using a direct current as in the method of Claim 1.

Lei discloses forming a chip bonding pad 12, for example from copper or aluminum in an upper portion of an uppermost dielectric insulating layer 10. (Col. 2, lines 56–64.) However, what follows the chip bonding pad 12 is not a pulse plating layer nor a direct current copper plated layer as in Claim 1, but instead, a single or multiple layer passivation coating 14 that leaves an opening 12A over the chip bonding pad 12 is applied. (Col. 3, lines 10–18.) The passivation coating 14 includes, for example, at least one of silicon nitride, polyimide, Benzocyclobutene, silicon dioxide, and silicon oxynitride. The opening area 12A is filled with

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metallization (UBM) layers, for example at least a lowermost layer of titanium 16A is blanket deposited to a thickness of from about 500 Angstroms to about 1500 Angstroms. A lowermost layer of titanium is preferred due to its superior stability and adhesion to the underlying passivation layer 14 and the copper bonding pad 12. (Col. 3, lines 19–27.) Therefore, Lei does not disclose a method for forming a bump pad by pulse plating on an electroless copper plating layer followed by electrolytic copper plating using a direct current on the pulse plated layer as in the method of Claim 1.

Finally, Beica et al. discloses a bump pad 102 formed on a semiconductor substrate, wherein the bump pad 102 is formed typically by physical vapor deposition (PVD) such as sputtering. (Para. [0060]). Following this, a passivation layer 104 is formed over the interconnect bump pads 102 leaving an opening, wherein the opening is filled by an under bump metallization (UBM) structure 106. The UBM structure may be deposited by PVD, such as sputtering or evaporation, or CVD processes. The UBM structure may be a composite structure, in order, a bottom chrome layer, a copper layer, and an upper tin layer. (Paras. [0061] to [0062].) Therefore, all three references of Lee, Lei, and Beica et al. have different methods for forming the *bump pad*, and none discloses the same sequence of steps for forming a bump pad as in the method of Claim 1.

Accordingly, even having consideration for all three disclosures of Lee, Lei and Beica et al., there is no teaching or even a suggestion for subjecting the electroless copper plating layer of Lei to pulse plating followed by electrolytic copper plating using a direct current to provide a bump pad having an electroless copper plated layer juxtaposed on an insulating layer, a pulse plated layer juxtaposed on the electroless copper plated layer, and a direct current copper plated layer juxtaposed on the pulse plated layer.

Accordingly, the withdrawal of the rejection of Claims 1-6 is respectfully requested.

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